SYLLABUS

1. Information about the program

1.1 Higher education institution	UNIVERSITY POLITEHNICA OF TIMISOARA
1.2 Faculty[1]/ Department [2]	ELECTRONICS, TELECOMUNICATON AND INFORMATION TECHNOLOGIES/EA
1.3 Field of study (name/code[3])	ELECTRONIC ENGINEERING, TELECOMUNICATION AND INFORMATION TECHNOLOGIES
1.4 Study cycle	License
1.5 Study program (name/code/qualification)	TST-ENG/20/20/10/100/10/TST-ENG

2. Information about the discipline

2.1 Name of discipline/ formative category[4]	Digital VLSI Design Techniquesf						
2.2 Coordinator (holder) of course activities	Jivet Ioan						
2.3 Coordinator (holder) of applied activities[5]	Jivet Ioan						
2.4 Year of study[6]	4	**2.5** Semester	7	**2.6** Type of evaluation	E	**2.7** Regime of discipline[7]	DO

3. Total estimated time – hours / semester: direct teaching activities (fully assisted or partly assisted) and individual training activities (unassisted) [8]

3.1 Number of fully assisted hours / week	5 of which:	**3.2** course	3	**3.3** seminar / laboratory / project	2
3.1* Total number of fully assisted hours / semester	70 of which:	**3.2*** course	42	**3.3*** seminar / laboratory / project	28
3.4 Number of hours partially assisted / week	0 of which:	**3.5** training	0	**3.6** hours for diploma project elaboration	0
3.4* Total number of hours partially assisted / semester	0 of which:	**3.5*** training	0	**3.6*** hours for diploma project elaboration	0
3.7 Number of hours of unassisted activities / week	3.93 of which:	additional documentary hours in the library, on the specialized electronic platforms and on the field			0.93
		hours of individual study after manual, course support, bibliography and notes			1.5
		training seminars / laboratories, homework and papers, portfolios and essays			1.5
3.7* Number of hours of unassisted activities / semester	55 of which:	additional documentary hours in the library, on the specialized electronic platforms and on the field			13
		hours of individual study after manual, course support, bibliography and notes			21
		training seminars / laboratories, homework and papers, portfolios and essays			21
3.8 Total hours / week [9]	8,93				
3.8* Total hours /semester	125				
3.9 Number of credits	5				

4. Prerequisites (where applicable)

4.1 Curriculum	• Basic Digital Circuits , Introductory HDL Knowledge

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[1] The name of the faculty which manages the educational curriculum to which the discipline belongs
[2] The name of the department entrusted with the discipline, and to which the course coordinator/holder belongs.
[3] The code provided in HG - on the approval of the Nomenclature of fields and specializations / study programs, annually updated.
[4] Discipline falls under the educational curriculum in one of the following formative disciplines: Basic Discipline (DF), Domain Discipline (DD), Specialist Discipline (DS) or Complementary Discipline (DC).
[5] Application activities refer to: seminar (S) / laboratory (L) / project (P) / practice/training (Pr).
[6] Year of studies in which the discipline is provided in the curriculum.
[7] Discipline may have one of the following regimes: imposed discipline (DI) or compulsory discipline (DOb)-for the other fundamental fields of studies offered by UPT, optional discipline (DO) or optional discipline (Df).
[8] The number of hours in the headings 3.1 *, 3.2 *, ..., 3.8 * is obtained by multiplying by 14 (weeks) the number of hours in headings 3.1, 3.2, ..., 3.8. The information in sections 3.1, 3.4 and 3.7 is the verification keys used by ARACIS as: (3.1) + (3.4) ≥ 28 hours / wk. and (3.8) ≤ 40 hours / wk.
[9] The total number of hours / week is obtained by summing up the number of hours in points 3.1, 3.4 and 3.7.

4.2 Competencies	• -

5. Conditions (where applicable)

5.1 of the course	• Videoprojector, Internet conection
5.2 to conduct practical activities	• FPGA Boards, Electronic Basic Tools

6. Specific competencies acquired through this discipline

Specific competencies	• Mastering HDL – VHDL and Verilog, design of Complex Digital Circuits
Professional competencies ascribed to the specific competencies	• Application of knowledge, concepts and basic methods related to computer system architecture, microprocessors, microcontrollers, programming languages and techniques.
Transversal competencies ascribed to the specific competencies	• Adaptation to new technologies, professional and personal development through continuous training, using printed documentation sources, specialized software and electronic resources in Romanian and at least one foreign language.

7. Objectives of the discipline (based on the grid of specific competencies acquired - pct.6)

7.1 The general objective of the discipline	• Understand the concepts behind high performance computing architectures required for the processing of the high volume of data in intelligent systems. Understand the concepts for data protection in complex architecture that ensure the safety requirements for automotive software design
7.2 Specific objectives	• Good understanding of high performance computing cores. Good understanding of Multi-processor system and on-chip communication infrastructure. Good understanding of memory organization and protection. Good understanding of GPUs and data parallel processing.

8. Content [10]

8.1 Course	Number of hours	Teaching methods [11]
L1. VHDL - Behavior to Structure Level of Abstract (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l1	3	Slides, discussion
L2. VHDL Simulation (Event Driven Procedure (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l2 + Sim_ro = CV) Extra 1. Finite state machines	3	
L3. VHDL Synthesis (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l9-10) Extra 2. Special Constructs VHDL - process ()	3	

(intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l1 + Capitolul2- CV) Extra 3. FPGA Internal Structures (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l4)		
L4. Verilog (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l6)	3	
L5. RISC Microprocessor basics (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l8)	3	
L6.VHDL Analog Mixed Signal (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l5)	3	
L7. Organizing Memory (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l7)	3	
L8. ARM processor and RISC V basics (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l14)	3	
L9. CMOS Technology.Fabrication (intranet.etc.upt.ro/~VHDL_ENG/lectures/l_1,2)	3	
L10. CMOS Technology.Devices (intranet.etc.upt.ro/~VHDL_ENG/lectures/l_3,4)	3	
L11. CMOS Technology.ICsample (intranet.etc.upt.ro/~VHDL_ENG/lectures/l_5,6,7)	3	
L12. Touch Technology (CV)	3	
L13. HDL Digital Recap (intranet.etc.upt.ro/~VHDL_ENG/2013pi/l_pi/l_13)	3	
L14. Special Topics (CV)	3	

Bibliography [12]   1 VHDL Cookbook, Univ Adeleide, Au 2009, OnLine resources.
2. I Jivet Proiectarea sistemelor digitalle utilizind descrieri HDL, 2009 Orizonturi Universitare.

8.2 Applied activities [13]	Number of hours	Teaching methods
Lab1. Basic VHDL Constructs (EVITA)		Exercises
Lab2. Structural Desciption in VHDL (Vivado - codes -inv_dff CC)		
Lab3. Structure inv_dff Simulation (Vivado)		
Lab4. Test_bench Construct in VHDL Vivado (codes in CV)		
Lab5. Picoblaze Structure and Codes (Vivado - codes in CV)		
Lab6. VHDL Synthesis (lecture notes)		
Lab7. Altera NIOS Processor (Altera Quartus - + CV presentation)		
Lab8. Verilog (EVITA Verilog)		
L9.Vivado HLS		

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[12] At least one title must belong to the discipline team and at least one title should refer to a reference work for discipline, national and international circulation, existing in the UPT library.
[13] Types of application activities are those specified in footnote 5. If the discipline contains several types of applicative activities then they are sequentially in the lines of the table below. The type of activity will be in a distinct line as: "Seminar:", "Laboratory:", "Project:" and / or "Practice/training".

(Internet Tutorial doc)		
Bibliography [14]		

9. **Corroboration of the content of the discipline with the expectations of the main representatives of the epistemic community, professional associations and employers in the field afferent to the program**

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10. **Evaluation**

Type of activity	10.1 Evaluation criteria [15]		10.2 Evaluation methods	10.3 Share of the final grade
10.4 Course			Exam	66%
10.5 Applied activities	**S:**			
	L:		Activity	34%
	P[16]:			
	Pr:			
10.6 Minimum performance standard (minimum amount of knowledge necessary to pass the discipline and the way in which this knowledge is verified [17])				
- 5 for couse exam and 5 for project work				

Date of completion	**Course coordinator (signature)**	**Coordinator of applied activities (signature)**
10.07.2023		

Head of Department (signature)	**Date of approval in the Faculty Council [18]**	**Dean (signature)**
	14.09.2023	

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[14] At least one title must belong to the discipline team.
[15] Syllabus must contain the procedure for assessing the discipline, specifying the criteria, methods and forms of assessment, as well as specifying the weightings assigned to them in the final grade. The evaluation criteria shall be formulated separately for each activity foreseen in the curriculum (course, seminar, laboratory, project). They will also refer to the forms of verification (homework, papers, etc.)
[16] In the case where the project is not a distinct discipline, this section also specifies how the outcome of the project evaluation makes the admission of the student conditional on the final assessment within the discipline.
[17] It will not explain how the promotion mark is awarded.
[18] The endorsement is preceded by the discussion of the board's view of the study program on the discipline record.